

ABSTRACT

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A method of fabricating a III-V heterostructure semiconductor device.

The method includes the steps of forming at least one conductive post overlying  
5 a semiconductor region to form a structure, encapsulating the structure and the  
conductive post to form a planarized cured passivation layer, and exposing the  
conductive post through the planarized cured passivation layer to form the  
semiconductor device.